

A cross-sectional view of a semiconductor device 100. The device features a substrate 102 with a central region 112 and two side regions 108a and 108b. A central layer 120c is positioned on the central region 112, and two side layers 120a and 120b are positioned on the side regions 108a and 108b, respectively. A top layer 114 is positioned on the central layer 120c. A bottom layer 104 is positioned on the substrate 102. The central region 112 is defined by a central opening 110. The side regions 108a and 108b are defined by side openings 106a and 106b, respectively. The central layer 120c and side layers 120a and 120b are shown with hatching patterns.

A cross-sectional view of a semiconductor device 200. The device features a substrate 202 with a central region 210. A central layer 220c is positioned on the substrate 202, flanked by two side layers 220a and 220b. A top layer 214 is deposited over the central region 210. The device is surrounded by a trench 204. The trench 204 is defined by a bottom surface 208a and 208b, and a side surface 206a and 206b. The central region 210 is also labeled with 212.

FIG. 3

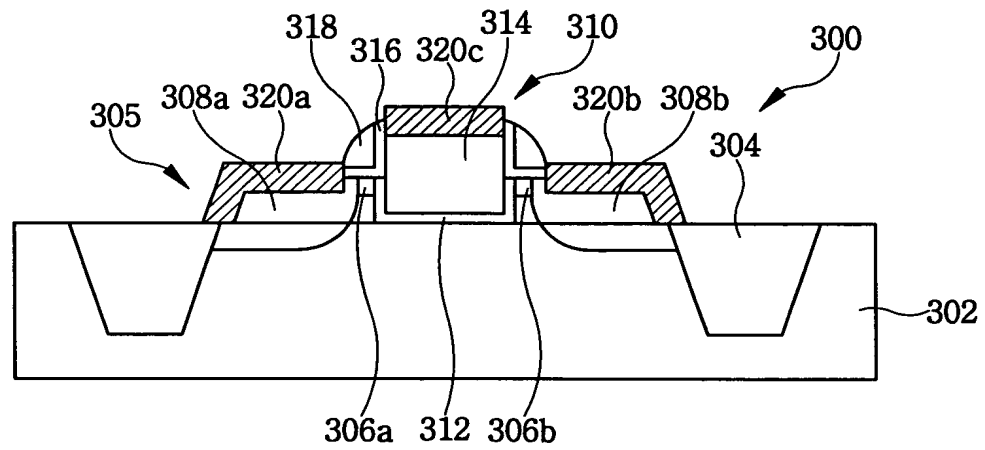


FIG. 4

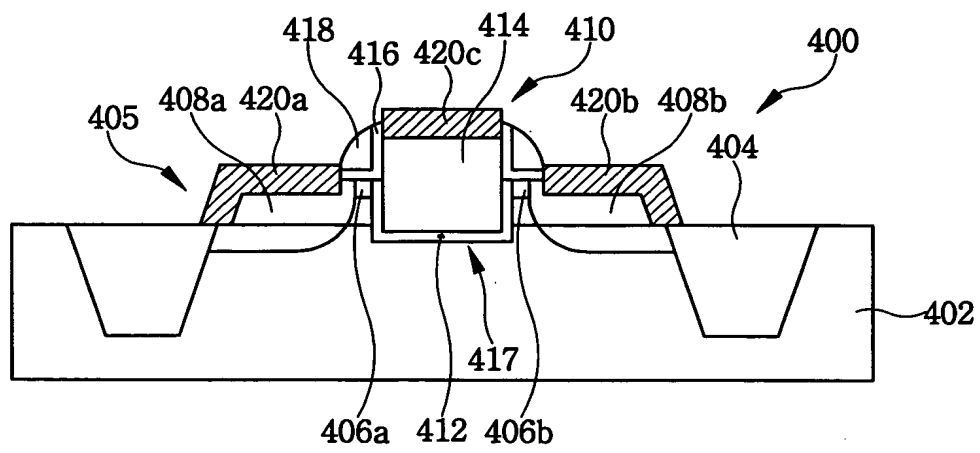


FIG. 5

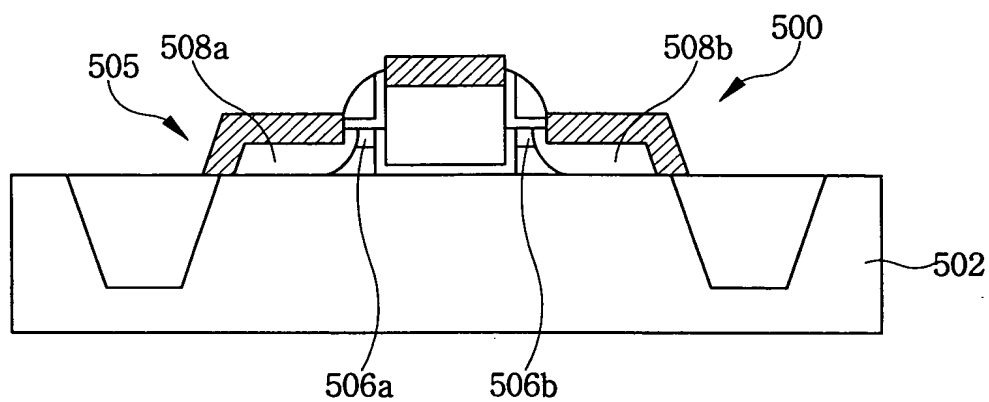


FIG. 6

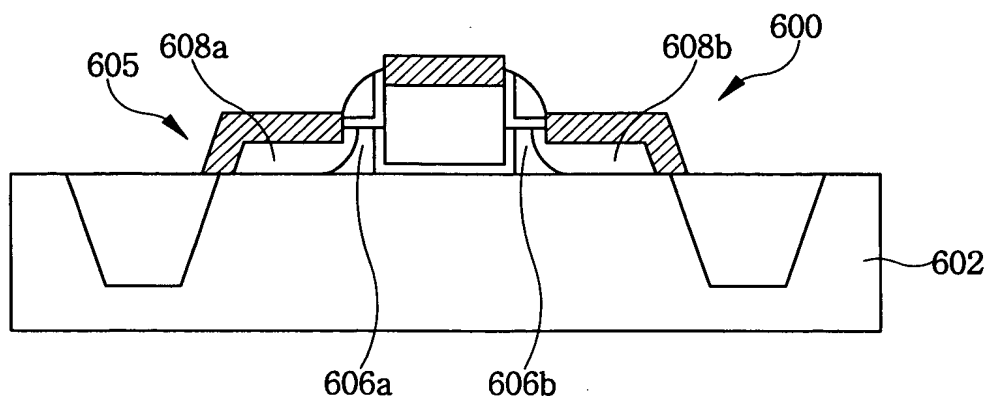


FIG. 7

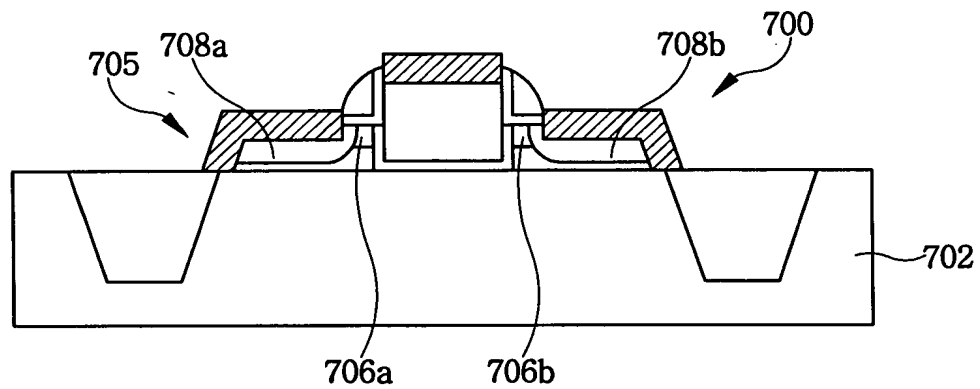


FIG. 8A

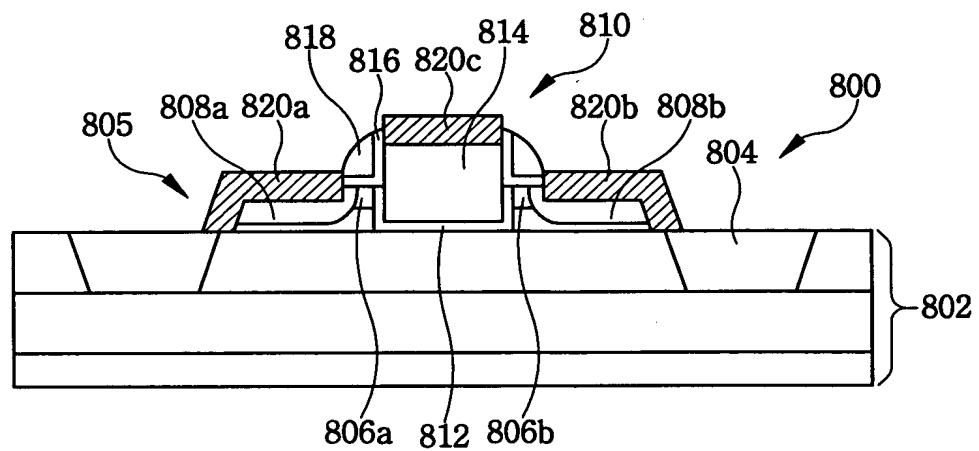


FIG. 8B

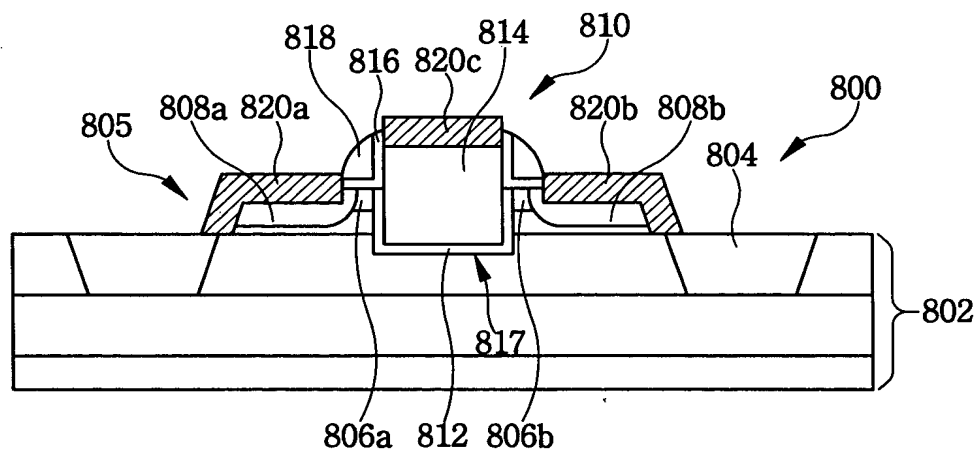


FIG. 9A

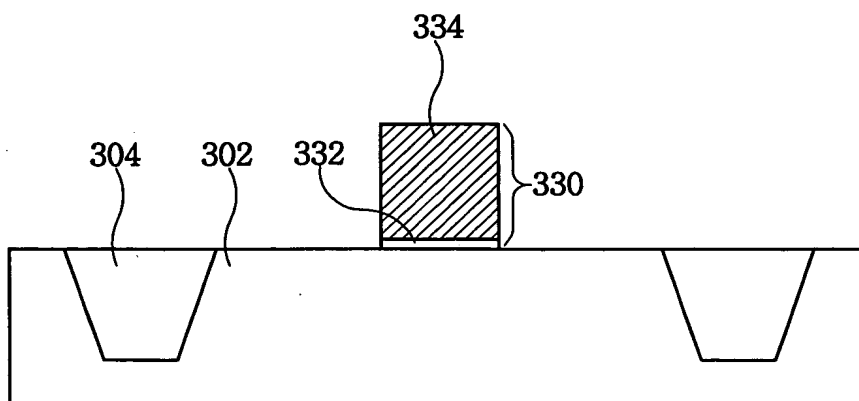


FIG. 9B

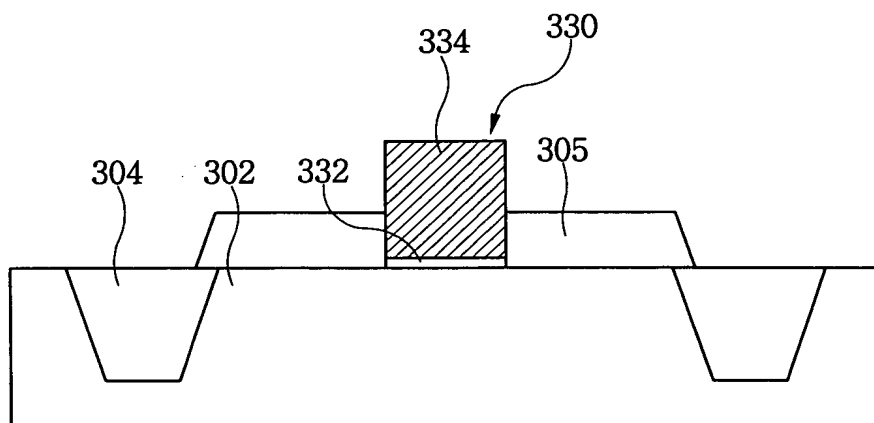


FIG. 9C

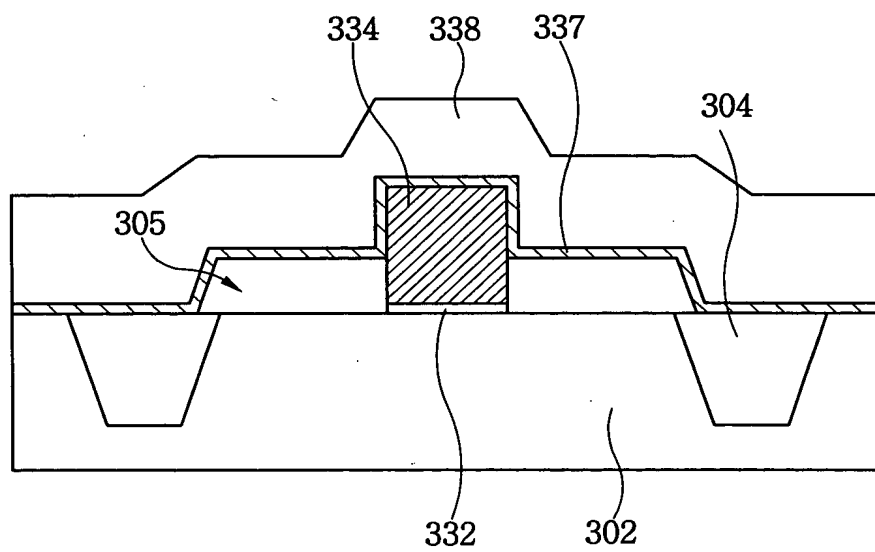


FIG. 9D

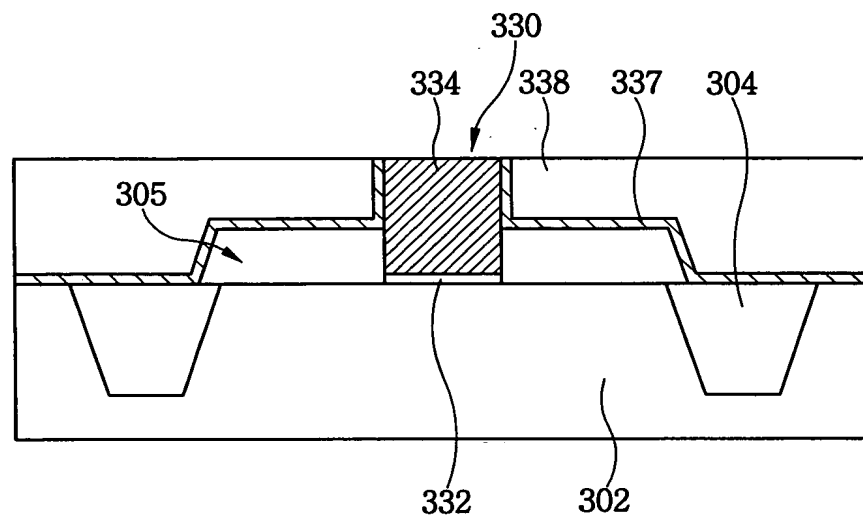


FIG. 9E

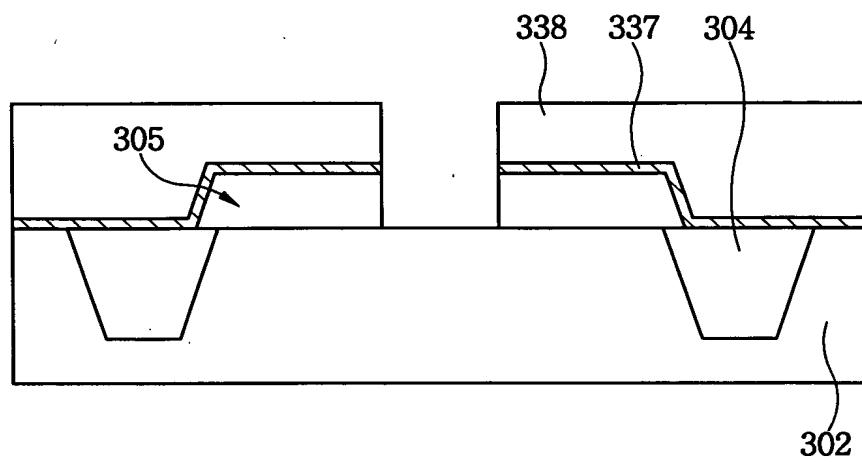


FIG. 9F

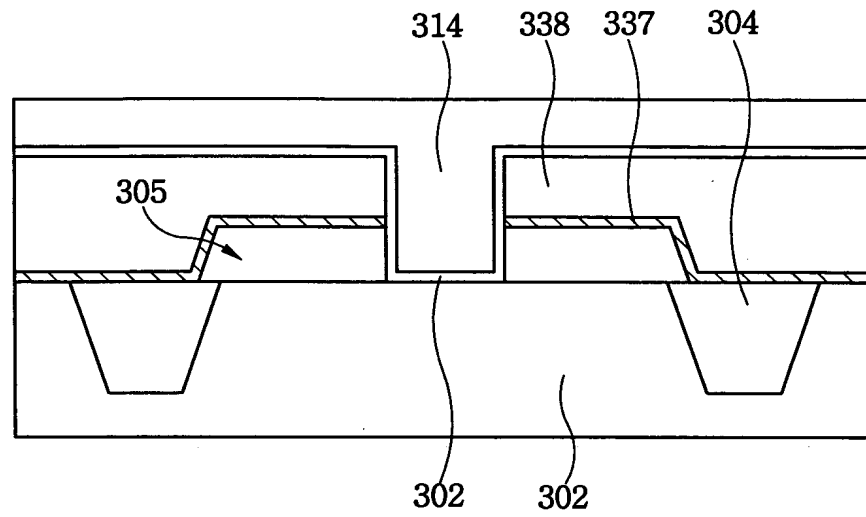


FIG. 9G

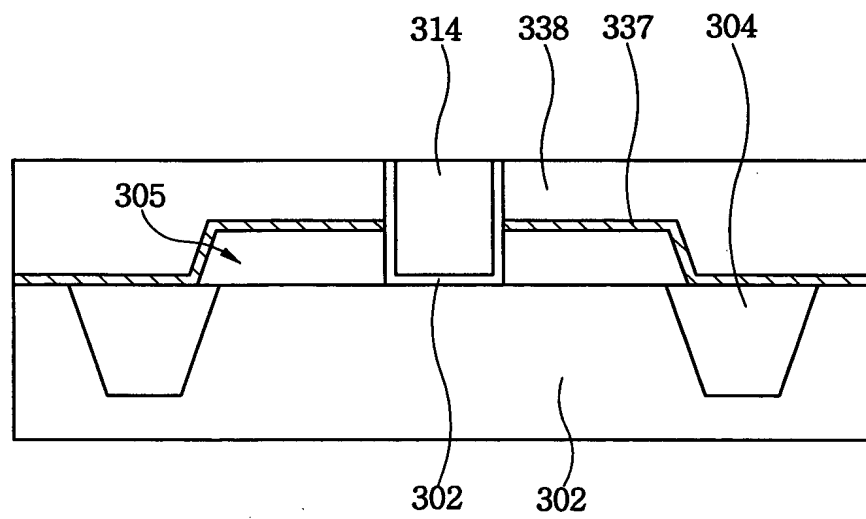




FIG. 9H

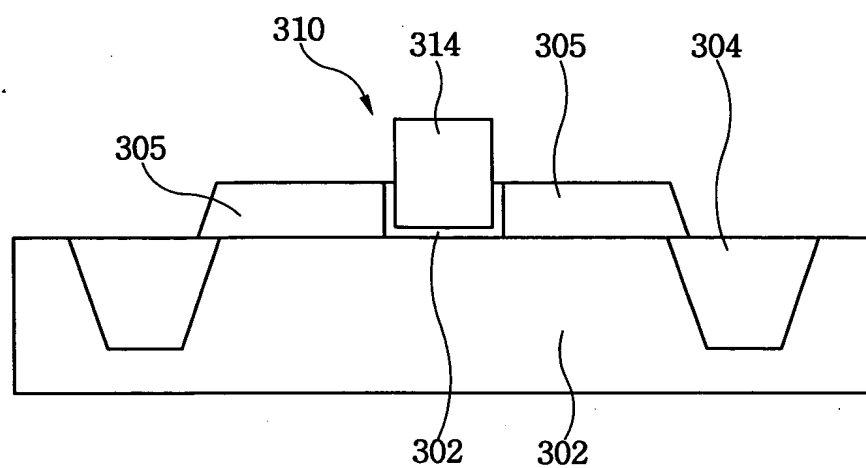


FIG. 9I

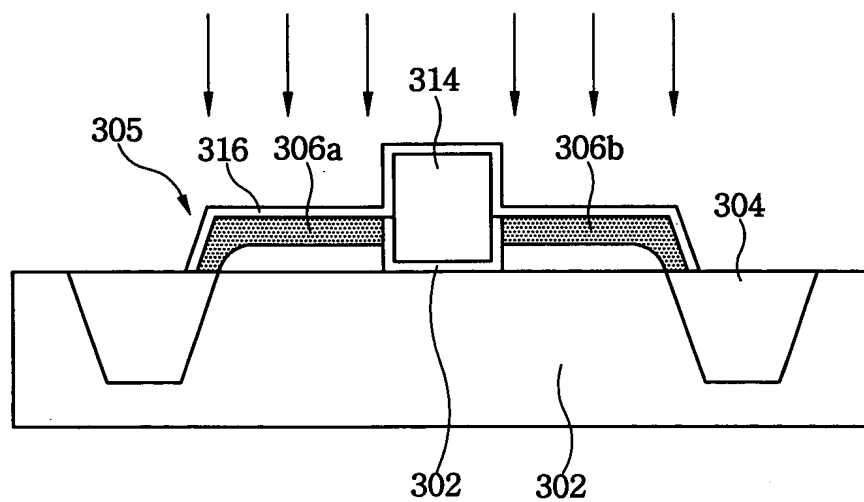


FIG. 9J

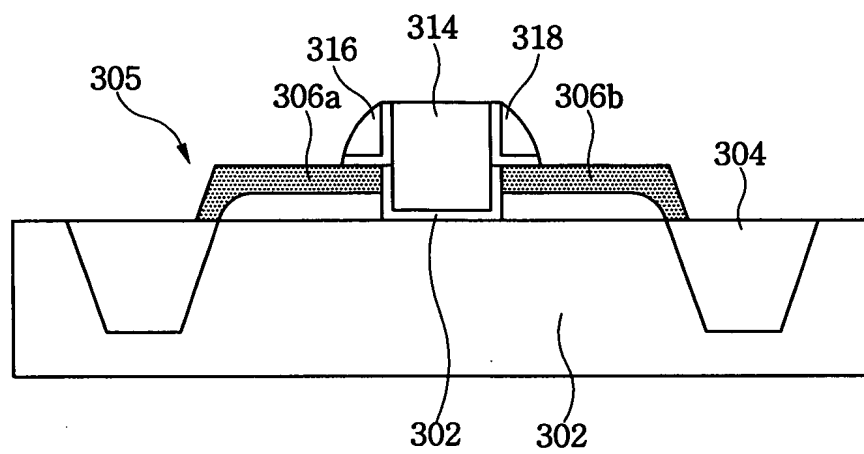


FIG. 9K

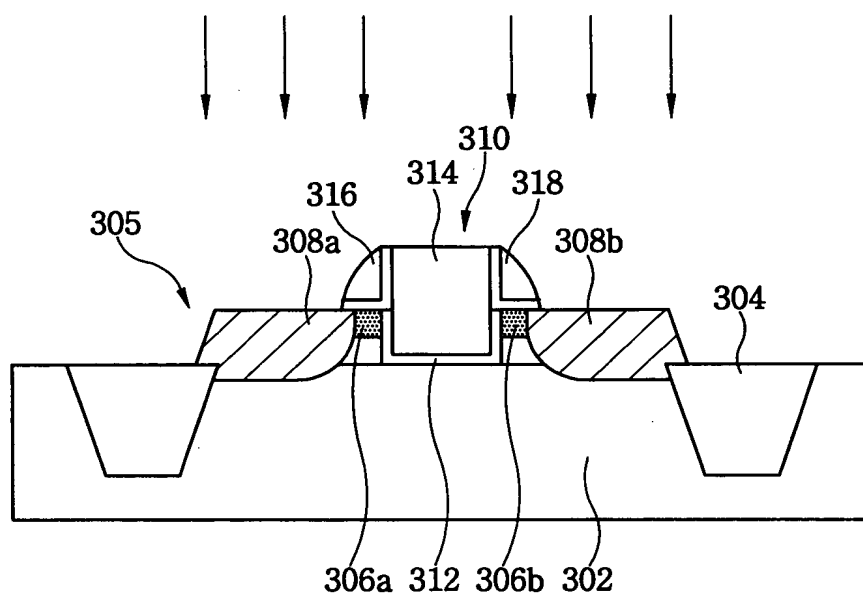


FIG. 9L

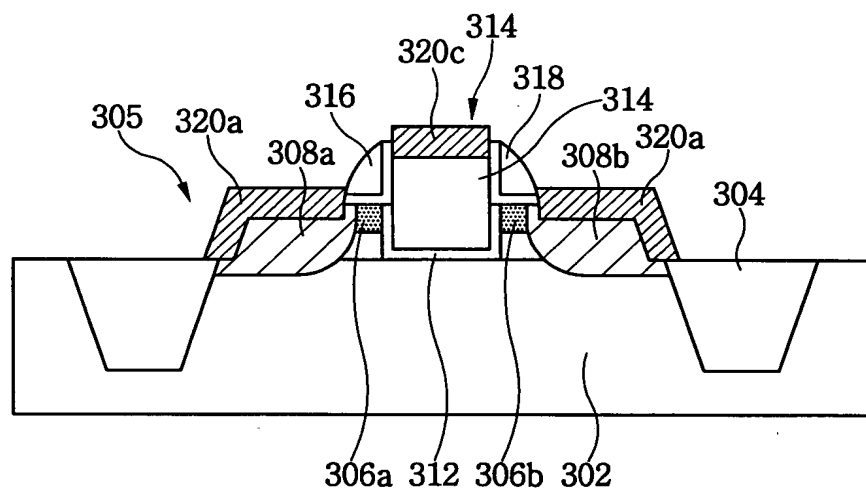


FIG. 10A

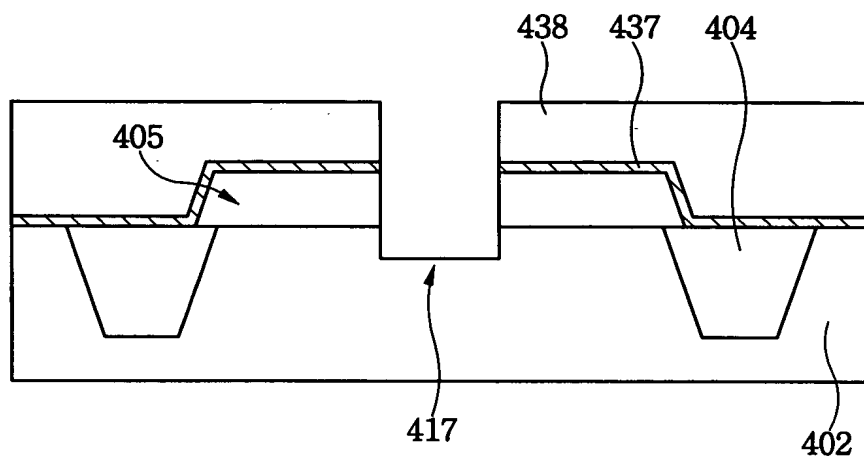


FIG. 10B

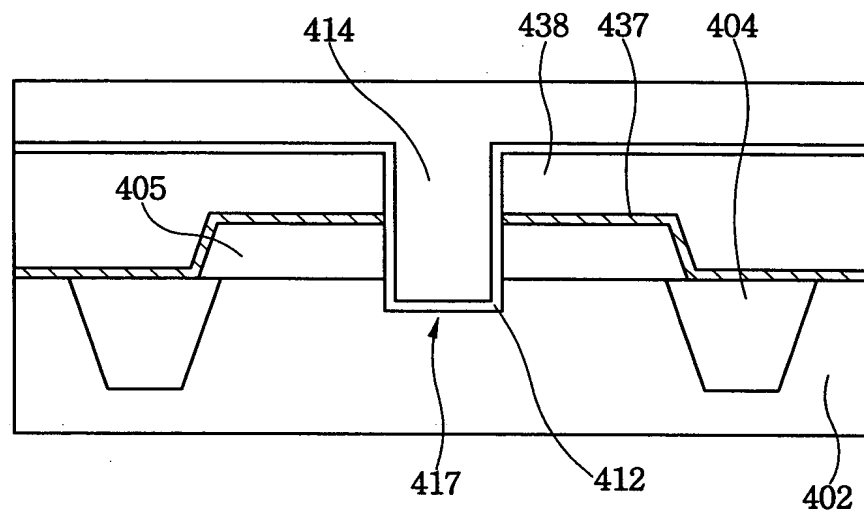


FIG. 10C

